WHAT IS CLAIMED IS:

1. A method for determining a cracking threshold for a dielectric material on a substrate comprising the steps of:

forming two or more test structures on the substrate, each test structure comprising two metal structures separated by the dielectric material having a width which is different for each test structure; and

determining whether the dielectric material between the two metal structures for each test structure has cracked during processing, the cracking threshold being approximately equal to the largest width of dielectric material that is cracked.

2. The method as recited in claim 1, wherein the step of determining whether the dielectric material between the two metal structures for each test structure has cracked during processing is performed by electrically probing the two metal structures in each test structure to measure a leakage current across the width of the dielectric material for each test structure.

3. The method as recited in claim 1, wherein the step of determining whether the dielectric material between the two metal structures for each test structure has cracked during processing is performed by optically inspecting the width of the dielectric material for each test structure.

4. The method as recited in claim 1, wherein the dielectric material is a low-k dielectric material chosen from the group consisting of polymide, silicon oxycarbide, hydrogen silsesquioxane, methyl silsesquioxane, bezocyclobutene, fluorinated glass, fluorinated aromatic ether, and inter-penetrated spin-on glass.

5. A test pattern for determining a cracking threshold for a dielectric material on a substrate comprising:

two or more test structures disposed on the substrate;

each test structure comprising two metal structures separated by the dielectric material having a width which is different for each test structure; and

wherein the cracking threshold is approximately equal to the largest width of dielectric material that is cracked after processing.

6. The test pattern as recited in claim 5, wherein the dielectric material is a low-k dielectric material chosen from the group consisting of polymide, silicon oxycarbide, hydrogen silsesquioxane, methyl silsesquioxane, bezocyclobutene, fluorinated glass, fluorinated aromatic ether, and inter-penetrated spin-on glass.

7. The test pattern as recited in claim 5, wherein the two metal structures are copper.

8. The test pattern as recited in claim 5, further comprising a barrier layer surrounding each metal structure.

9. The test pattern as recited in claim 5, wherein each metal structure comprises a damascene structure containing a metal.

10. The test pattern as recited in claim 5, wherein the test structures are disposed on more than one layer of a silicon-on-insulator structure.

11. The test pattern as recited in claim 5, wherein the width is within a range of 0.05 and 1.0 μm.

12. The test pattern as recited in claim 5, wherein the width of the dielectric material for the two or more test structures differs by approximately 0.05 μm.

13. The test pattern as recited in claim 5, further comprising a sealing ring disposed around each test structure.

14. The test pattern as recited in claim 13, wherein the separation between the sealing ring and the two metal structures exceeds the width.

15. The test pattern as recited in claim 5, wherein each test structure comprises:

two or more test substructures; and

each test substructure includes two metal structures having a first width which is different for each test substructure, the two metal structures separated by the dielectric material having a second width which is substantially constant for each test substructure and different for each test structure.

16. The test pattern as recited in claim 15, wherein the first width is selected from a range of 1 to 30 μm and the second width is selected from a range of 0.05 to 1.0 μm.

17. The test pattern as recited in claim 15, wherein the two or more test substructures are arranged in a pyramid pattern.

18. The test pattern as recited in claim 15, wherein:

the first width for the first test substructure, second test substructure, third test substructure, fourth test substructure and fifth test substructure is approximately 3, 5, 10, 15 and 20 μm, respectively; and

the second width for the first test structure, second test structure, third test structure, fourth test structure, fifth test structure, sixth test structure, seventh test structure, eighth test structure, ninth test structure, tenth test structure, eleventh test structure and twelfth test structure is approximately 0.1, 0.2, 0.25, 0.3, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, and 0.8 μm, respectively.

19. A test pattern comprising:

two or more test structures disposed on a substrate;

each test structure includes two or more test substructures; and

each test substructure comprising a sealing ring, two metal structures having a first width which is different for each test substructure, and a dielectric material disposed between each metal structure and the sealing ring and between the two metal structures, the dielectric material between the two metal structures having a second width which is substantially constant for each test substructure and different for each test structure.

20. The test pattern as recited in claim 19, wherein the dielectric material is a low-k dielectric material chosen from the group consisting of polymide, silicon oxycarbide, hydrogen silsesquioxane, methyl silsesquioxane, bezocyclobutene, fluorinated glass, fluorinated aromatic ether, and inter-penetrated spin-on glass.

21. The test pattern as recited in claim 19, wherein the two metal structures are copper.

22. The test pattern as recited in claim 19, further comprising a barrier layer surrounding each metal structure.

23. The test pattern as recited in claim 19, wherein each metal structure comprises a damascene structure containing a metal.

24. The test pattern as recited in claim 19, wherein the test structures are disposed on more than one layer of a silicon-on-insulator structure.

25. The test pattern as recited in claim 19, wherein the first width is selected from a range of 1 to 30 μm and the second width is selected from a range of 0.05 to 1.0 μm.

26. The test pattern as recited in claim 19, wherein the second width of the dielectric material for the two or more test structures differs by approximately 0.05 μm.

27. The test pattern as recited in claim 19, wherein the separation between the sealing ring and the two metal structures exceeds the second width.

28. The test pattern as recited in claim 19, wherein the two or more test substructures are arranged in a pyramid pattern.

29. The test pattern as recited in claim 19, wherein:

the first width for the first test substructure, second test substructure, third test substructure, fourth test substructure and fifth test substructure is approximately 3, 5, 10, 15 and 20 μm, respectively; and

the second width for the first test structure, second test structure, third test structure, fourth test structure, fifth test structure, sixth test structure, seventh test structure, eighth test structure, ninth test structure, tenth test structure, eleventh test structure and twelfth test structure is approximately 0.1, 0.2, 0.25, 0.3, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, and 0.8 μm, respectively.